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| Faculty of Engineering & Technology | | | |
| Ramaiah University of Applied Sciences | | | |
| Department | Computer Science and Engineering | Programme | B. Tech. |
| Semester/Batch | 3rd /2018 | | |
| Course Code | 19CSC205A | Course Title | Microprocessors and Assembly Programming |
| Course Leader | P.Padma Priya Dharishini , Supriya M.S. | | |

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| Assignment - 1 | | | | | | | | |
| Name of Student | | |  | Register No | |  | | |
| Sections |  | Marking Scheme | | | Max Marks | | First Examiner Marks | Second Examiner Marks |
| Part-A | A1.1 | Assembly Language Program | | | 3 | |  |  |
| A1.2 | Clock cycle time, Execution time of sequence recognizer, CPI | | | 3 | |  |  |
| A1.3 | AMAT | | | 2 | |  |  |
| A1.4 | Comparison of Execution time | | | 2 | |  |  |
|  | **Max Marks** | | | **10** | |  |  |

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| **Course Marks Tabulation** | | | | |
| **Component- CET B Assignment** | **First Examiner** | **Remarks** | **Second Examiner** | **Remarks** |
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|  |  |  |  |  |
|  |  |  |  |  |
| **Marks (out of 10 )** |  |  |  |  |
| Signature of First Examiner Signature of Second Examiner | | | | |

**Please note:**

1. Documental evidence for all the components/parts of the assessment such as the reports, photographs, laboratory exam / tool tests are required to be attached to the assignment report in a proper order.
2. The First Examiner is required to mark the comments in RED ink and the Second Examiner’s comments should be in GREEN ink.
3. The marks for all the questions of the assignment have to be written only in the **Component – CET B: Assignment** table.
4. If the variation between the marks awarded by the first examiner and the second examiner lies within +/- 3 marks, then the marks allotted by the first examiner is considered to be final. If the variation is more than +/- 3 marks then both the examiners should resolve the issue in consultation with the Chairman BoE.

**Assignment – 1**

**Term-1**

**Instructions to students:**

1. The assignment consists of 1 question.
2. Maximum marks is 10.
3. The assignment has to be neatly word processed as per the prescribed format.
4. The maximum number of pages should be restricted to 4.
5. The printed assignment must be submitted to the subject leader.
6. **Submission Date: 25th OCT 2019**
7. **Submission after the due date is not permitted.**
8. **IMPORTANT**: It is essential that all the sources used in preparation of the assignment must be suitably referenced in the text.
9. Marks will be awarded only to the sections and subsections clearly indicated as per the problem statement/exercise/question

**Preamble:**

This course is intended to provide a thorough knowledge of the concepts and components of computer organisation and architecture to students using modern microprocessors as case studies. It introduces the architecture and operation of CPU, memory and I/O. The students are also exposed to assembly language programming, modern computing systems and their scope for engineering applications.

**Problem Statement:**

Consider a Sequence Recognizer (SR) that accepts strings of bits as an input. SR asserts its output when it recognizes target bit sequence. In this assignment, students have to design SR that accepts any string of bits as input and output goes to 1 when it recognizes target bit sequence 1011(binary) in its input. SR keeps checking for the input bit sequence and does not reset when it recognizes target bit sequence.

Sample input and output:

Input = 0010110110

Output = 0000010010

Document the following:

* Develop an assembly language program to implement the given sequence recognizer.
* Calculate Clock cycle time, Execution time of sequence recognizer, Clock cycles Per-Instruction (CPI) based on parameters given in Table 1.
* Calculate Average Memory Access Time (AMAT) taken by sequence recognizer based on the parameters given by Table 2.
* Find out the execution time taken by the developed sequence recognizer by executing it. Compare observed execution time with calculated execution time. Comment on the results.

Table 1: Clock cycle taken by different types of instructions

|  |  |  |  |
| --- | --- | --- | --- |
| Instruction type | Source 1 | Source 2 /Destination | Number of Clock cycles |
| Arithmetic and logical instructions | Register | Register | 1 |
| Immediate | Register | 1 |
| Register | Memory | 7 |
| Memory | Register | 7 |
| Data transfer instructions | Register | Register | 1 |
| Immediate | Register | 1 |
| Register | Memory | 7 |
| Memory | Register | 7 |
| Conditional Instructions | ---- | ---- | 5 |

Table 2: Cache configuration

|  |  |  |
| --- | --- | --- |
| Parameters | L1 cache | L2 cache |
| Associativity | 2-way set Associative | 4-way set Associative |
| Block size | 32 bytes | 64 bytes |
| Cache size | 512 Kb | 1Gb |
| Hit rate | 40% | 60% |
| Miss Penalty | 7 | 30 |
| Hit time | 4 ns | 20 ns |

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